IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A frequency shift keyed (FSK) receiver capable of demodulating an incoming transmitted signal comprising:

a phase-locked loop for receiving an oscillator reference signal having a reference frequency ~~F1~~ and generating a reference carrier frequency signal having a desired frequency ~~N1(F1), wherein N1 may be a non-integer value~~, said phase-locked loop comprising:

a phase detector having a first input for receiving said oscillator reference signal and a second input; and

a frequency divider circuit for dividing an actual frequency of said reference carrier frequency signal by an adjustable integer value ~~N2~~ applied to a control input of said frequency divider circuit to thereby generate a feedback signal applied to said second input of said phase detector;

a frequency discriminator that receives said incoming transmitted signal and said reference carrier frequency signal and generates a correction signal corresponding to a difference between a center frequency of said incoming transmitted signal and said actual frequency of said reference carrier frequency signal; and

a delta-sigma modulator controlled by said correction signal operable to generate a sequence of integers having an average value ~~of N1~~ over a defined time period, wherein said sequence of integers are applied to said control input of said frequency divider circuit.

2. (Original) The FSK receiver as set forth in Claim 1 further comprising a subtraction circuit capable of subtracting said correction signal from a nominal carrier frequency value to thereby generate a control frequency signal that controls said delta-sigma modulator.

3. (Currently Amended) The FSK receiver as set forth in Claim 1 wherein the frequency discriminator comprises a first mixer that receives said incoming transmitted signal and said reference carrier frequency signal and generates an intermediate frequency signal having a frequency equal to a difference between said center frequency of said incoming transmitted signal and said actual frequency of said reference carrier frequency signal.

4. (Currently Amended) The FSK receiver as set forth in Claim 3 wherein the frequency discriminator further comprises a signal splitter that splits said intermediate frequency signal into a first child intermediate frequency signal and a second child intermediate frequency signal.

5. (Currently Amended) The FSK receiver as set forth in Claim 4 wherein the frequency discriminator further comprises a delay element that delays said second child intermediate frequency signal ~~, T~~.

6. (Currently Amended) The FSK receiver as set forth in Claim 5 wherein said delay ~~, T,~~ is [[a]] substantially equal to a quarter wavelength of said second child intermediate frequency signal.

7. (Currently Amended) The FSK receiver as set forth in Claim 5 wherein the frequency discriminator further comprises a second mixer that receives said first child intermediate frequency signal and said time-delayed second child intermediate frequency signal and generates a direct current ("DC") correction voltage.

8. (Original) The FSK receiver as set forth in Claim 7 wherein said frequency discriminator further comprises an analog-to-digital converter that receives said DC correction voltage and outputs said correction signal.

9. (Currently Amended) A method of demodulating a transmitted signal comprising the steps of:

mixing the transmitted signal and a reference carrier frequency signal having a desired frequency ~~N1(F1), wherein N1 may be a non-integer value,~~ produced by a phase-locked loop (PLL) to generate a correction signal corresponding to a difference between a center frequency of the transmitted signal and an actual frequency of the reference carrier frequency signal;

in the phase-locked loop (PLL), dividing the actual frequency of the reference carrier frequency signal by an adjustable integer value ~~N2~~ applied to a control input of a frequency divider circuit to generate a PLL feedback signal ~~having a frequency of (N1/N2)F1~~;

in the phase-locked loop, comparing ~~the~~ a phase of an oscillator reference signal having a reference frequency ~~F1~~ and ~~the~~ a phase of the PLL feedback signal and using ~~the~~ a phase difference to control a voltage controlled oscillator generating the reference carrier frequency signal having the desired frequency ~~N1(F1)~~; and

using a delta-sigma modulator controlled by the correction signal to generate a sequence of integers having an average value ~~of N1~~ over a defined time period, wherein the sequence of integers are applied to the control input of the frequency divider circuit.

10. (Original) The method as set forth in Claim 9 further comprising the step of subtracting the correction signal from a nominal carrier frequency value to thereby generate a control frequency signal that controls the delta-sigma modulator.

11. (New) The FSK receiver of Claim 1, wherein:

the reference frequency has a frequency of F1;

the average value has a value of N1;

the desired frequency has a frequency of N1*F1; and

the adjustable integer value has a value of N2.

12. (New) The FSK receiver of Claim 11, wherein N1 represents a non-integer value.

13. (New) The method of Claim 9, wherein mixing the transmitted signal and the reference carrier frequency signal comprises:

generating an intermediate frequency signal having a frequency equal to a difference between the center frequency of the transmitted signal and the actual frequency of the reference carrier frequency signal.

14. (New) The method of Claim 13, wherein mixing the transmitted signal and the reference carrier frequency signal further comprises:

splitting the intermediate frequency signal into a first child intermediate frequency signal and a second child intermediate frequency signal.

15. (New) The method of Claim 14, wherein mixing the transmitted signal and the reference carrier frequency signal further comprises:

delaying the second child intermediate frequency signal.

16. (New) The method of Claim 15, wherein mixing the transmitted signal and the reference carrier frequency signal further comprises:

mixing the first child intermediate frequency signal and the time-delayed second child intermediate frequency signal to generate a direct current ("DC") correction voltage.

17. (New) The method of Claim 16, wherein mixing the transmitted signal and the reference carrier frequency signal further comprises:

converting the DC correction voltage into a digital value; and

outputting the digital value as the correction signal.

18. (New) An apparatus, comprising:

an antenna capable of receiving an incoming transmitted signal; and

a receiver capable of demodulating the incoming transmitted signal, the receiver comprising:

a phase-locked loop capable of receiving an oscillator reference signal and generating a reference carrier frequency signal, the phase-locked loop comprising:

a phase detector having a first input and a second input, the first input capable of receiving the oscillator reference signal; and

a frequency divider capable of dividing an actual frequency of the reference carrier frequency signal based on a control signal applied to a control input of the frequency divider to generate a feedback signal applied to the second input of the phase detector;

a frequency discriminator capable of receiving the incoming transmitted signal and the reference carrier frequency signal and generating a correction signal corresponding to a difference between a center frequency of the incoming transmitted signal and the actual frequency of the reference carrier frequency signal; and

a delta-sigma modulator controlled by the correction signal and capable of generating the control signal applied to the control input of the frequency divider.

19. (New) The apparatus of Claim 18, wherein the frequency discriminator comprises:

a first mixer capable of receiving the incoming transmitted signal and the reference carrier frequency signal and generating an intermediate frequency signal having a frequency equal to the difference between the center frequency of the incoming transmitted signal and the actual frequency of the reference carrier frequency signal;

a signal splitter capable of splitting the intermediate frequency signal into a first child intermediate frequency signal and a second child intermediate frequency signal;

a delay element capable of delaying the second child intermediate frequency signal;

a second mixer capable of receiving the first child intermediate frequency signal and the time-delayed second child intermediate frequency signal and generating a direct current ("DC") correction voltage; and

an analog-to-digital converter capable of receiving the DC correction voltage and outputting the correction signal.

20. (New) The apparatus of Claim 19, wherein the delay element is capable of delaying the second child intermediate frequency signal for a delay period that is substantially equal to a quarter wavelength of the second child intermediate frequency signal.